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# METHOD AND APPARATUS FOR PROVIDING SYNCHRONIZATION IN A CIRCUIT SWITCHED TIME DIVISION MULTIPLEXED NETWORK

## Technical Field of Invention

The present invention refers to a method and an apparatus for providing synchronization in a circuit switched time division multiplexed network, wherein data are transferred on bitstreams, each bitstream being divided into recurrent frames, each frame being divided into time slots and being defined by recurrent frame synchronization information provided in one or more of said time slots.

## Technical Background and Prior Art

Today, new types of circuit-switched communication networks are being developed for the transfer of information using synchronous or isochronous, time division multiplexed bitstreams, wherein each bitstream is divided into regularly recurrent frames, or cycles, each frame in turn being divided into time slots.

An example of such a network is described in "The DTM Gigabit Network", Christer Bohm, Per Lindgren, Lars Ramfelt, and Peter Sjödin, Journal of High Speed Networks, 3(2):109-126, 1994, and in "Multi-gigabit networking based on DTM", Lars Gauffin, Lars Håkansson, and Björn Pehrson, Computer networks and ISDN Systems, 24(2):119-139, April 1992.

Generally, on each bitstream, a trigger node arranged at an uppermost upstream location on the bitstream is provided to write a regularly recurrent frame synchronization pattern into one or more time slots on the bitstream, thereby establishing frame synchronization on said bitstream for downstream provided nodes to synchronize their operations to.

When forming a network comprising several links or bitstreams, these are connected using so called switch

nodes. Since the bitstreams transfer synchronous or isochronous communication in a TDM fashion, the frame rate of the different network bitstreams need to be synchronized in order to avoid problems such as loss of data (also known in the art as "slip").

This is generally provided by a synchronization plan and arrangement that ensures the same frame repetition frequency on all communication bitstreams in the network. Such a synchronization arrangement is typically a hierarchical synchronization structure of the kind described in EP 522 607 A1, using two types of synchronization nodes: so called synchronization master nodes and synchronization slave nodes. Each such synchronization master or slave node controls at least one outgoing bitstream, which means that it is responsible for generating frames and clock signals on the respective bitstreams. In this way, a frame synchronization signal or pattern, initially provided by the synchronization master node, is propagated via the synchronization slave nodes in a tree-like fashion through the network. The synchronization master node thus dictates the frame frequency of the network. There will be a propagation delay at the slave node from the point in time when it receives the frame synchronization pattern from its master node until the synchronization slave node starts its frame on the bitstream(s) that it controls, but this delay is constant and does not interfere with the synchronization. In this way a synchronization tree is built up that propagates the frame start synchronization to all bitstreams.

A disadvantage with these prior art schemes is that they allow little freedom as to the construction, build up and configuration of the network, requiring the use of a very strict, top-down hierarchy. Also, limitations as to network management during link failures, re-establishment of link synchronization, and the like, apply correspondingly.

An object of the invention is therefore to provide simple scheme for achieving network synchronization which allows greater freedom as to the construction, build up and configuration of the network, as well as to network management during link failures, re-establishment of link synchronization, and the like.

Summary of the invention

The above mentioned and other objects of the invention are achieved by the invention as defined in the accompanying claims.

Hence, according to a first aspect of the invention, there is provided a method of the kind mentioned in the introduction, said method being characterized by the steps of: detecting recurrent frame synchronization information on a bitstream of said network, said recurrent frame synchronization information being derived from a frame synchronization providing node of said network; generating data relating to the frame synchronization established by said detected recurrent frame synchronization information; and transmitting said data to said frame synchronization providing node of said network, said data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon.

Correspondingly, according to a second aspect of the invention, there is provided an apparatus of the kind mentioned in the introduction, characterized by: means for detecting recurrent frame synchronization information on a bitstream of said network, said recurrent frame synchronization information being derived from a frame synchronization providing node of said network; means for generating data relating to the frame synchronization established by said detected recurrent frame synchronization information; and means for transmitting said data to said frame synchronization providing node of said network

network, said data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon.

Hence, the invention provides for a node connected to a bitstream of the network to send feedback information related to the frame synchronization situation, typically at the location of the node, to a so called trigger node, generally arranged at a location upstream with respect to said node, said trigger node controlling, directly or indirectly (via an intermediate trigger node), the establishment of frame synchronization, defined by frame synchronization information, for example in the form of a frame synchronization pattern defining for example the start of each respective frame, on said bitstream.

Vice versa, the invention provides for a trigger node, arranged to establish frame synchronization on a bitstream by transmitting frame synchronization information thereto, to control the establishment of frame synchronization on said bitstream, either directly or indirectly (via an intermediate trigger node), based upon frame synchronization detection data provided by, or via, one or more nodes typically connected to said network at a location downstream with respect to said trigger node.

In fact, if desired, a node connected to a bitstream at a location downstream with respect to a trigger node providing the frame synchronization information, such as a trigger pattern, on said bitstream may be arranged to actually control the frame rate on said bitstream by repeatedly instructing the trigger node, in a master-slave type of relationship, on how or when to provide the trigger pattern.

An advantage of the invention is that it allows for greater freedom when designing the network configuration by providing a mechanism which advantageously makes it possible to circumvent or at least lighten the prior art

requirement of a strict hierarchical top-down synchronization control and distribution scheme.

According to a preferred embodiment of the invention, as taken in the context of a switch node arranged to switch time slot data between a first bitstream and a second bitstream of said network, a frame drift between said first and said second bitstream is determined, said frame drift defining said data relating to the frame synchronization established by said recurrent frame synchronization information. Said data relating to said frame drift is then transmitted to one or more frame synchronization providing nodes of said network, said frame drift data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon for eliminating said frame drift.

Consequently, the invention very advantageously makes it possibly to interconnect two or more network sections, wherein each network section has its frame synchronization provided by its own frame synchronization master node.

In prior art, this would not be possible, since frame synchronization is required to be distributed in a hierarchical top-down tree like fashion in order to ensure synchronization consistency throughout the network. The use of two independent master nodes would inevitably lead to frame drift between different parts of the network, consequently causing data slip or data congestion, since it is practically impossible to provide to master nodes operating at the exact same bit rate and frame frequency.

However, according to the invention, by continuously informing one or both of the frame synchronization master nodes of the frame drift situation, preferably taken at the point where the two networks sections are interconnected, this information may then be used to continuously

adjust the frame frequency established by the master nodes so that any frame drift tendency is continuously eliminated.

As is understood, this aspect of the invention in a fundamental way provides for greater freedom as to the construction, build up and configuration of the network, as well as to network management during link failures, re-establishment of link synchronization, and the like.

Preferably, said data relating to the frame synchronization situation are transmitted to said at least one frame synchronization providing node of said network using one or more time slots of one or more bitstreams of said network. Although an alternative wherein a communication system being external to said network may also be used to transmit said data, the alternative of using the network itself for this transmission provides a simple and preferred channel of communication.

Furthermore, the controlling of the transmission of said recurrent frame synchronization information preferably comprises controlling the size of one or more frames of a bitstream of said network. Also, the size of one or more frames is preferably controlled by adjusting the number of slots provided within one or more frames, for example the number of fill slots, also called guard band slots, provided to said one of more frames. According to another alternative, the frame size may also be controlled by controlling the bit rate used within said one or more frames, for example by controlling a bit clock or counter used at the synchronization providing node.

According to a preferred embodiment, the controlling of the transmission of said recurrent frame synchronization information comprises controlling or adjusting the operation of a phase locked loop (PLL), which synchronizes the operation at the synchronization providing node, based upon said data.

As is understood, said data, typically when relating to the frame drift between two bitstreams, may also be used to inform the trigger node of one of the bitstreams in case of a link failure, or the like, with respect to the other bitstream.

Also, as understood by those skilled in the art, the features of the invention are readily realized using conventional electronic circuitry and/or network software tools.

Furthermore, the invention is preferably used, although not limited thereto, in a so called DTM (Dynamical Synchronous Transfer Mode) network, wherein the time slots of each frame of a bitstream are divided into two groups: control slots, used for control signaling between nodes of the network, and data slots, used for the transfer of user data between end users connected to said nodes. Typically, in such a network, each node has access to at least one control slot and to a dynamic number of data slots on the bitstream used by said node, wherein the number of data slots allocated to each node is changed dynamically based upon the transfer capacity requested by the end users served by the respective node.

It is to be noted that said recurrent frame synchronization information may be provided in many different forms. For example, in the preferred embodiment, as will be described in detail below with reference to the drawings, the recurrent frame synchronization information is provided in the form of a preferably regularly recurring frame synchronization pattern, said pattern as such, i.e. by its mere location in the bitstream, defining each frame of a bitstream, for example by being located at the start of each frame. However, in another embodiment, said recurrent frame synchronization information does not need to define the frame location by the its mere location in the bitstream. Instead, its the content or "message" of the information that provides data as to the timing of one or more frames of the bitstream, for example provi-

ding data as to where (or rather when) each of the next ten frames starts and/or ends.

Further aspects, advantages, and features of the invention will be more fully understood from the following detailed description of exemplifying embodiments thereof.

## Brief Description of the Drawings

Exemplifying embodiments of the invention will now be described with reference to the accompanying drawings, wherein:

Figs. 1-4 schematically show bitstreams of a circuit switched time division multiplexed network operating according to the invention;

Fig. 5 schematically shows the configuration of a bitstream of the kind shown in Figs. 1 to 4;

Figs. 6a and 6b schematically show frame synchronization situation with respect to a first and a second bitstream; and

Fig 7 schematically shows a network node according to an embodiment of the invention.

## Detailed Description of Preferred Embodiments

The configuration of a simple circuit switched time division multiplexed network 10a operating according to the invention will now be described with reference to Fig. 1. The network 10a in Fig. 1 comprises two separate bitstreams B1 and B2 propagating in the directions indicated by arrows in Fig. 1 and hence transferring data in opposite directions between nodes 12-18 of the network. The nodes provide network access to end users connected to the respective node.

On bitstream B1, the first, uppermost provided node 12 is arranged to provide frame synchronization by transmitting a regularly recurrent frame synchronization pattern, referred to below as "trigger pattern", and a regularly recurrent guard pattern to bitstream B1, indi-

cating the start and end, respectively, of each frame (cf. Fig. 5).

Similarly, on bitstream B2, the uppermost provided node 18 is arranged to provide frame synchronization by transmitting corresponding trigger and guard patterns to bitstream B2, indicating the start and end, respectively, of each frame.

In this embodiment, the node 12 acts as a so called synchronization master node, referred to below as "master node", whereas the node 18 acts as a so called synchronization slave node, referred to below as "slave node". In this context, this means that the node 18 will transmit its trigger pattern to the bitstream B2 in synchronization with the received trigger pattern provided by the master node 12 on bitstream B1.

Consequently, the intermediate nodes 14 and 16 synchronizes their network access operations according to the trigger pattern provided on bitstream B1 when transmitting data to or receiving data from bitstream B1, and according to the trigger pattern provided on bitstream B2 when transmitting data to or receiving data from bitstream B2.

In the embodiment shown in Fig. 1, and according to the invention, the node 16 is arranged to use, e.g., one time slot per frame on bitstream B2 to transmit data, relating to the timing of the reception of the trigger pattern on bitstream B1, to the master node 12. This information is then received by the master node 12 and used at the master node 12 as a basis for determining how to control the provision of the trigger pattern on bitstream B1. If, for example, the data provided by the node 16 suggests that it would be desirable to lower the network frame rate, the master node 12 may decide to increase the number of time slots included in the guard band in each frame on bitstream B1, thereby increasing the length of each frame on bitstream B1 (and consequently on bitstream B2 due to the master slave relationship between

the master node 12 and the slave node 18). There may be many different reasons for the node 16 to suggest an increase or decrease in the frame rate. For example, data congestion in the operation of the end users served by the node 16, or rate changes in another network also connected to the node 16. In fact, if desired, the node 16 may act as the "true" master node of the network, repeatedly instructing the master node 12 on how to increase or decrease the bitstream frame rate.

The configuration of another circuit switched time division multiplexed network 10b operating according to the invention will now be described with reference to Fig. 2. The network 10b is an expansion of the network 10a in Fig. 1, and further description of those features already described with reference to Fig. 1 is therefore omitted.

In Fig. 2, the network 10b comprises, in addition to those parts already described above, two bitstreams B3 and B4 propagating in directions indicated by corresponding arrows and hence transferring data in opposite directions between nodes 16, 20-16 of the network.

Hence, on bitstream B3, the uppermost provided node 16 is arranged to provide frame synchronization by transmitting corresponding trigger and guard patterns to bitstream B3, indicating the start and end, respectively, of each frame. Similarly, on bitstream B4, an upstream provided node (not shown) is arranged to provide frame synchronization by transmitting trigger and guard patterns thereto, indicating the start and end, respectively, of each frame.

In Fig. 2, the node 16, as well as the node 18, acts as a synchronization slave node in relation to the master node 12. In this context, this means that the node 16 will transmit a trigger pattern to the bitstream B3 in synchronization with the received trigger pattern provided by the master node 12 on bitstream B1. Also the node (not shown) providing the trigger pattern to bitstream B4

will act as a slave node to the slave node 16, i.e. the provision of the trigger pattern on bitstream B4 will be governed by the provision of the trigger pattern on bitstream B3, which in turn will be governed by the provision of the trigger pattern on bitstream B1.

In the embodiment shown in Fig. 2, the node 16 is still arranged to use, e.g., one time slot per frame on bitstream B2 to transmit data, relating to frame rate synchronization situation on bitstreams B3 and B4, typically in relation to the frame rate synchronization situation on bitstreams B1 and B2, to the master node 12. This information is then received by the master node 12 and used at the master node 12 as a basis for determining how to control the provision of the trigger pattern on bitstream B1, in similar to what has already been described with reference to Fig. 1. If, for example, the data derived by the node 16 and provided to the master node 12 states that, due to some reason or another, there is a difficulty in keeping the frame rate on bitstreams B3 and B4 up to speed with the frame rate on bitstreams B1 and B2, the master node 12 may decide to increase the number of time slots included in the guard band in each frame on bitstream B1, thereby increasing the length of each frame and thus decreasing the network frame rate.

Also, each one of the nodes 20-26 may be arranged to transmit similar data relating to the frame rate to the node 16 (or directly to the master node 12 via the node 16, the latter then acting as switch node) in a similar manner as described above.

The configuration of another circuit switched time division multiplexed network 10c operating according to the invention will now be described with reference to Fig. 3. The network 10c is an expansion of the network 10b in Fig. 2, and further description of those features already described with reference to Fig. 2 is therefore omitted.

In Fig. 3, the network 10c comprises, in addition to those parts already described above, four bitstreams B5, B6, B7, and B8 propagating in directions indicated by corresponding arrows and hence transferring data in pair-wise opposite directions between nodes 24, 30, 32, 34 and 42, 44, 34, 26, respectively, of the network.

In similar to what has been described with reference to Figs. 1 and 2, the node 24 in Fig. 3 is arranged to provide frame synchronization on bitstream B5 by transmitting corresponding trigger and guard patterns thereto. Also, on bitstream B6, an upstream provided node (not shown) is arranged to provide frame synchronization on bitstream B6 by transmitting trigger and guard patterns thereto. Similarly, the node 42 is arranged to provide frame synchronization on bitstream B7 by transmitting corresponding trigger and guard patterns thereto. On bitstream B8, an upstream provided node (not shown) is arranged to provide frame synchronization on bitstream B6 by transmitting trigger and guard patterns thereto.

In Fig. 3, the node 24, as well as the node 16, acts as a synchronization slave node in relation to the master node 12. In this context, this means that the node 24 will transmit a trigger pattern to the bitstream B5 in synchronization with the received trigger pattern provided by the slave node 16 on bitstream B3, which in turn is provided in synchronization with the trigger pattern provided by the slave node 12 on bitstream B1.

However, on bitstream B7, the node 42 will act as a synchronization master node and is hence not arranged to transmit the trigger pattern to bitstream B7 based upon the timing of any incoming trigger pattern received at the node 42.

Instead, in the embodiment shown in Fig. 3, the switch node 34 is arranged to detect the trigger pattern provided on bitstream B5, as well as the trigger pattern provided on bitstream B7, and to determine the occurrence of any frame drift between the two bitstreams. If so, the

switch node 34 will use, e.g., one time slot per frame on bitstream B8 to transmit data stating, e.g., the polarity and magnitude of any occurring frame drift to the node 42. This information is then received by the node 42 and used at the node 42 as a basis for determining how to control the provision of the trigger pattern on bitstream B7 in order to ensure frame synchronization consistency over the network, more specifically at the location of the switch node 34. Consequently, if, for example, the bit rate generated locally at the master node 12 differs somewhat compared to the bit rate generated locally at the node 42, this difference is compensated for by, e.g., the increasing or decreasing of the frame length on bitstream B7, for example as achieved by the increasing or decreasing of the number of guard band time slots provided by the master node 42 to each frame of the bitstream B7 or by the adjustment of a phase locked loop controlling the operation within the node 42..

As is understood, the frame drift information could just as well be transmitted from the switch node 34 to the master node 12, said master node 12 then taking care of the frame drift problem and letting the node 42 continue its operation unaffected.

The configuration of another circuit switched time division multiplexed network 10d operating according to the invention will now be described with reference to Fig. 4. The network 10d is an expansion of the network 10b in Fig. 3, and further description of those features already described with reference to Fig. 1 is therefore omitted.

In Fig. 4, the network 10d comprises, in addition to those parts already described above, two bitstreams B9 and B10 propagating in directions indicated by correspon-ding arrows and hence transferring data in opposite directions between nodes 28, 36, 38, and 40.

The node 28 is arranged to provide frame synchroni-zation on bitstream B9 and a corresponding node (not

shown) is arranged to provide frame synchronization on bitstream B10. The node 28, in similar to node 24, acts as a synchronization slave node in relation to the master node 12 (via the slave node 16).

In Fig. 4, the switch node 34 and the switch node 40 are arranged to detect the occurrence of any frame drift between bitstream B7 and bitstream B5 and between bitstream B7 and bitstream B9, respectively. The switch nodes 34, 40 will then use, e.g., one time slot each per frame on bitstream B8 to transmit data stating, e.g., the polarity and magnitude of any occurring frame drifts to the node 42. This information is then received by the node 42 and used at the node 42 as a basis for determining how to control the provision of the trigger pattern on bitstream B7 in order to ensure, in the best way possible, frame synchronization consistency over the network, more specifically at the location of the both switch nodes 34 and 40.

Here also, the frame drift information could just as well be transmitted from the switch nodes 34 and 40 to the master node 12, said master node 12 then taking care of the frame drift problem and letting the operation at node 42 continue unaffected.

The configuration of a bitstream of the kind transferred on the bitstreams shown in Figs. 1-4 will now be described with reference to Fig. 5. As shown in Fig. 5, each bitstream is divided into regularly recurrent cycles or frames having a generally fixed length, for example 125 μs. Each frame is in turn divided into fixed size, for example 64 bits, time slots. The number of time slots within a frame depends on the network's bit rate.

The time slots are in general divided into two groups, control slots C and data slots D. The control slots C are used for control signaling between nodes of the network, i.e. for carrying messages between nodes for the internal operation of the network, such as for channel establishment, slot allocation, and the like. The

data slots D are used for the transfer of user data between end users connected to said nodes.

In addition to said control slots and data slots, each cycle comprises a frame synchronization pattern in the form of bit groups provided to define one or more synchronization slots S, as described above, used to synchronize the operation of each node in relation to each frame. Also, a guard pattern G comprising one or more slots is added at the end of each frame to facilitate frame synchronization.

Each node has access to at least one control slot C and to a dynamic number of data slots D on the bitstream used by said node. Each node uses its control slot C to communicate with other nodes within the network. The number of data slots D allocated to each node depends upon the transfer capacity requested by the end users served by the respective node. If the end users of a certain node require a large transfer capacity, the node will allocate more data slots for that purpose. On the other hand, if the end users of a certain node merely requires a small transfer capacity, the node may limit its number of allocated data slots. The allocation of time slots and data slots to different nodes may by dynamically adjusted as the network load changes.

Figs. 6a and 6b schematically show the frame synchronization situation at a switch node, in this case the switch node 34 in Figs. 3 and 4, operating in relation to the two schematically shown bitstreams B5 and B7. In Figs. 6a and 6b, each bitstream comprises a stream of time slots, and each frame is defined by a frame synchronization pattern comprising one time slot (marked as a black filled square in the figures). Also, one or more guard band time slots, illustrated as a hatched squares, are provided at the end of each frame.

In the situation shown in Fig. 6a, when a first trigger pattern on bitstream B5 is detected by the node 34, time slot number 356 is received by the node 34 on

bitstream B7. Then, as the next trigger pattern is detected on bitstream B5, time slot number 357 is received on bitstream B7, and so on. As a result, the node 34 determines that the frame length on bitstream B5 is longer than the frame length on bitstream B7 and that the frame drift is one time slot per frame. Information as to this frame drift situation is then transmitted, in a time slot on bitstream B8 in Fig. 3 or 4, to the node 42 controlling the frame rate on bitstream B7. Based upon this information, the node 42 will add an extra guard band time slot to each frame on bitstream B7 (as illustrated by the two guard band time slot in the bitstream B7 in Fig. 6b), thus eliminating the frame drift.

As a result, in Fig. 6b, after said change has taken place, at each detection of the recurrent trigger pattern on bitstream B5 by the node 34, the same time slot number 360 is received by the node 34 on bitstream B7. The node 34 then determines that the there is no frame drift at the moment and preferably transmits this information to the master node.

As is understood, the configuration of the bitstreams shown in Fig. 5, 6a and 6b, for example, the number of time slots included in the synchronization patterns and the guard patterns, is merely meant to be illustrative. Hence, the size of the frame drift compared to the frame length is very exaggerated and the actual number of time slots within each frame is normally far greater than the one shown. Furthermore, the synchronization pattern need not be a single contiguous set of time slots provided at the start of each frame, but may very well be provided in other forms and configurations.

En exemplifying embodiment of a node performing the operations discussed above will now be described with reference to Fig. 7. In Fig. 7, the node 100, which in this example is assumed to be the switch node 34 of Fig. 3, is connected to the bitstreams B5, B6 (not shown), B7 (not shown) and B8, and comprises a bitstream access unit

102, a bit clock locking circuit 104, an input demultiplexor 106, a time slot counter 108, a trigger control circuit 110, a bitstream access unit 112, a trigger generator 118, and a message generator 120.

In the node 100, time slot data, such as trigger patterns, control data for network signaling, user data, guard band fill slots, and the like, are received from the bitstream B5 via the bitstream access unit 102 and are supplied to the bit clock locking circuit 104 and the input demultiplexor 106. The bit clock locking circuit 104 locks the bit clock of the node to the clock rate received on the bitstream B5, so that the node will operate at a clock frequency corresponding to the one received on the bitstream B5. The bit clock locking circuit 104 provides the derived clock frequency to the time slot counter 108 (as well as to other circuits of the node which need provision of the clock frequency). Based upon the clock frequency derived by the bit clock locking circuit 104, the time slot counter 108 will count time slot numbers (each time slot comprising, e.g., 64 bits), typically starting from zero to essentially the frame length.

An output clock signal 114 from the time slot counter is provided to, among others, the input demultiplexor 106, the bitstream access unit 112 and the trigger control circuit 110. Based upon the clock signal 114, the input demultiplexor 106 will demultiplex the input bitstream bits into 64-bit time slot data groups which are sequentially provided to the trigger control circuit 110, the bitstream access unit 112, and the trigger generator 118 at the rate of the clock signal.

The function of the trigger control circuit 110 is to monitor that a trigger pattern is received on bitstream B7 within a predetermined time interval. When the trigger pattern is detected within said time interval, or if no trigger pattern has been detected within said time interval at the end thereof, the trigger control circuit

110 will reset 116 the counter, thus providing for the start of new frame of time slot data. The trigger or reset signal 116 is provided to the counter 108, the message generator 120 and the trigger generator 118.

The message generator 120 also receives a similar trigger signal on line 122 from a corresponding set of units (not shown) arranged within said node for providing access to bitstream B7. The trigger signal on line 122 will thus provide information as to the reception of a trigger pattern on bitstream B7 (preferably including information designating when no trigger pattern has been received within the said time interval, thus indicating some sort of link or node failure). The message generator 120 continuously compares the timings of the reception of the trigger signal 116 and the timings of the reception of the trigger signal 122. As an output, the message generator 120 generates time slot data which provide information as the occurrence of any frame drift between the two bitstreams B5 and B7 (or the occurence of, for example, a link or node failure). This time slot data is then transmitted, using the bitstream access unit 112, to a synchronization providing node typically attached to the bitstream B8 downstream with respect to the node 100.

Generally, the trigger generator 118 will generate a trigger pattern to be provided to the bitstream B8 via the bitstream access unit 122 either using the trigger signal 116, as shown in Fig. 7, or using a locally generated clock signal (not shown) as a reference. (Typically, as is understood, the trigger generator will use the trigger signal 116 as a reference when acting as an intermediate node or as a synchronization slave node, but will use a locally generated clock signal as a reference when acting as a synchronizatino master node).

In the latter case, i.e. when acting as a "head end" or frame synchronization providing node, in Fig. 7, the trigger generator 118 is provided to receive data relating to frame drift or the like from the bitstream B1 via

the input demultiplexor 106. Hence, the trigger generator 118 is provided to adjust the transmission of the trigger pattern to bitstream B8 in consideration of any frame drift data received from bitstream B5.

Hence, the functions provided by a) the frame synchronization monitoring message generator 120 and b) the frame drift message receiving trigger generator 118 basically embody two different aspects of the invention.

Although exemplifying embodiments of the invention have been described in detail above with reference to the accompanying drawings, the invention is of course not limited thereto. Consequently, as is understood by those skilled in the art, modifications, alterations, and combinations thereof will fall within scope of the invention, as defined by the accompanying claims.

## CLAIMS

1. Method for providing synchronization in a circuit switched time division multiplexed network, wherein data are transferred on bitstreams, each bitstream being divided into recurrent frames, each frame being divided into time slots and being defined by recurrent frame synchronization information provided in one or more of said time slots, said method comprising the steps of:

detecting recurrent frame synchronization information on a bitstream of said network, said recurrent frame synchronization information being derived from a frame synchronization providing node of said network;

generating data relating to the frame synchronization on said bitstream as defined by the detected recurrent frame synchronization information; and

transmitting said data to said frame synchronization providing node, said data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon.

2. Method as claimed in claim 1, wherein said data are transmitted to said frame synchronization providing node of said network using one or more time slots of one or more bitstreams of said network.

3. Method as claimed in claim 1 or 2, wherein said data are transferred using one or more time slots of a bitstream which transfers data in a direction opposite to that of said a bitstream.

4. Method as claimed in claim 1, 2, or 3, wherein the controlling of the transmission of said recurrent frame synchronization information comprises controlling the size of one or more frames of a bitstream of said network.

5. Method as claimed in claim 4, wherein said controlling of the size of one or more frames comprises controlling the number of slots provided in said one of more frames.

6. Method as claimed in claim 4, wherein said controlling of the size of one or more frames comprises controlling the bit rate of said one or more frames.

7. Method as claimed in any one of the preceding claims, wherein a switch node is arranged to switch time slot data between a first bitstream and a second bitstream of said network, said method comprising:

determining a frame drift between said first and said second bitstream, said frame drift defining said data relating to the frame synchronization as defined by said detected recurrent frame synchronization information; and

transmitting said data relating to said frame drift to at least said frame synchronization providing node of said network, said data preferably being used at said frame synchronization providing node for controlling the transmission of respective recurrent frame synchronization information based thereupon for eliminating said frame drift.

8. Method as claimed in claim 7, wherein said data relating to said frame drift are transferred using one or more time slots of at least one of the bitstreams of said network.

9. Method as claimed in claim 8, wherein said data relating to said frame drift are transferred using time slots of a third bitstream which transfers data in a direction opposite to that of said first and/or second bitstream.

10. Method as claimed in any one of the preceding claims, comprising the steps of:

receiving, at said frame synchronization providing node of said network, said data relating to the frame synchronization defined by said detected recurrent frame synchronization information; and

controlling the transmission of the recurrent frame synchronization information provided by said frame synchronization providing node based thereupon.

11. Method as claimed in any one of the preceding claims, wherein said recurrent frame synchronization information comprises a regularly recurrent frame synchronization pattern defining each frame of the respective bitstream.

12. Method for providing synchronization of a circuit switched time division multiplexed network, comprising the steps of:

providing, at a node of the network, a bitstream with recurrent frame synchronization information, said information defining recurrent frames on said first bit-stream, each frame being divided into time slots;

receiving data relating to the frame synchronization defined by said recurrent frame synchronization information as detected at another node of the network; and

controlling the transmission of said recurrent frame synchronization information based upon said received data.

13. Method as claimed in claim 12, wherein said data comprise phase drift data and wherein the control of the transmission of said recurrent frame synchronization information aims to eliminate said frame drift.

14. Method as claimed in claim 12 or 13, wherein said step of controlling the transmission of said recurrent frame synchronization information comprises controlling the frame rate on said a bitstream.

15. Method as claimed in claim 14, wherein said controlling of the frame rate comprises controlling the number of slots provided in one of more frames of said a bitstream.

16. Method as claimed in claim 14, wherein said controlling of the frame rate comprises controlling the bit rate of one or more frames of said a bitstream.

17. Method as claimed in any one of claims 12-16, wherein said data is received at said a node in one or more time slots of another bitstream which transfers data in a direction opposite to that of said a bitstream, said another bitstream also being divided into recurrent frames, each frame being divided into time slots.

18. Method as claimed in any one of claims 12-17, wherein said recurrent frame synchronization information comprises a regularly recurrent frame synchronization pattern defining each frame of the respective bitstream.

19. Apparatus for providing synchronization in a circuit switched time division multiplexed network, wherein data are transferred on bitstreams, each bit-stream being divided into recurrent frames, each frame being divided into time slots and being defined by recurrent frame synchronization information provided in one or more of said time slots, comprising:

means (110) for detecting recurrent frame synchronization information on a bitstream of said network, said recurrent frame synchronization information being derived

from a frame synchronization providing node of said network;

means (120) for generating data relating to the frame synchronization on said bitstream as defined by said detected recurrent frame synchronization information; and

means (112) for transmitting said data to said frame synchronization providing node of said network, said data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon.

20. Apparatus as claimed in claim 19, wherein said means for transmitting data are provided to transmit said data to said frame synchronization providing node of said network using one or more time slots of one or more bitstreams of said network.

21. Apparatus as claimed in claim 19 or 20, wherein said means for transmitting data are provided to transmit said data using one or more time slots of a bitstream which transfers data in a direction opposite to that of said a bitstream.

22. Apparatus as claimed in any one of claims 19 to 21, wherein said apparatus is arranged to switch data between a first and a second bitstream of said network, wherein:

said means for detecting recurrent frame synchronization information on a bitstream of said network is provided in the form of means for detecting recurrent frame synchronization information on said first and a second bitstream;

said means for generating data are provided in the form of means for determining a frame drift between said first and second bitstreams, said frame drift defining

said data relating to the frame synchronization as defined by said detected recurrent frame synchronization information; and

said means for transmitting said data are provided in the form of means for transmitting said data relating to said frame drift to at least said frame synchronization providing node of said network, said data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon for eliminating said frame drift.

23. Apparatus as claimed in claim 22, wherein said data relating to said frame drift are transferred using one or more time slots of at least one of the bitstreams of said network.

24. Apparatus as claimed in claim 23, wherein said data relating to said frame drift are transferred using time slots of a third bitstream which transfers data in a direction opposite to that of said first and/or second bitstream.

25. Apparatus as claimed in any one of claims 19-24, wherein said recurrent frame synchronization information comprises a regularly recurrent frame synchronization pattern defining each frame of the respective bitstream.

26. Apparatus for providing synchronization of a circuit switched time division multiplexed network, comprising:

means (112, 118) for providing, at a node or the network, a bitstream with recurrent frame synchronization information defining recurrent frames on said first bitstream, each frame being divided into time slots;

means (102, 106) for receiving data relating to the frame synchronization defined by said recurrent frame

synchronization information as detected at another node of the network; and

means (118) for controlling the transmission of said recurrent frame synchronization information into said a bitstream based upon or considering said data.

27. Apparatus as claimed in claim 26, wherein said data comprise phase drift data and wherein the control of the transmission of said recurrent frame synchronization information aims to eliminate said frame drift.

28. Apparatus as claimed in claim 26 or 27, wherein said means for controlling the transmission of said recurrent frame synchronization information comprises means for controlling the size of one or more frames of said a bitstream.

29. Apparatus as claimed in claim 28, wherein said means for controlling the transmission of said recurrent frame synchronization information comprises means for controlling the number of slots provided within said one of more frames of said a bitstream.

30. Apparatus as claimed in claim 28, wherein said means for controlling the transmission of said recurrent frame synchronization information comprises means for controlling the bit rate of one or more frames of said a bitstream.

31. Apparatus as claimed in any one of claims 26-30, wherein said data is received in one or more time slots of another bitstream which transfers data in a direction opposite to that of said first bitstream, said another bitstream also being divided into recurrent frames, each frame being divided into time slots.

32. Apparatus as claimed in any one of claims 26-31, wherein said recurrent frame synchronization information comprises a regularly recurrent frame synchronization pattern defining each frame of the respective bitstream.

## ABSTRACT

The present invention refers to a method and an apparatus for providing synchronization in a circuit switched time division multiplexed network, wherein data are transferred on bitstreams, each bitstream being divided into recurrent frames, each frame being divided into time slots and being defined by recurrent frame synchronization information provided in one or more of said time slots.

According to the invention, data relating to the timing of the detection of recurrent frame synchronization information are generated and transmitted to at least one frame synchronization providing node of said network, said data preferably being used at said frame synchronization providing node for controlling the transmission of said recurrent frame synchronization information based thereupon.

Elected for publication: Fig. 3

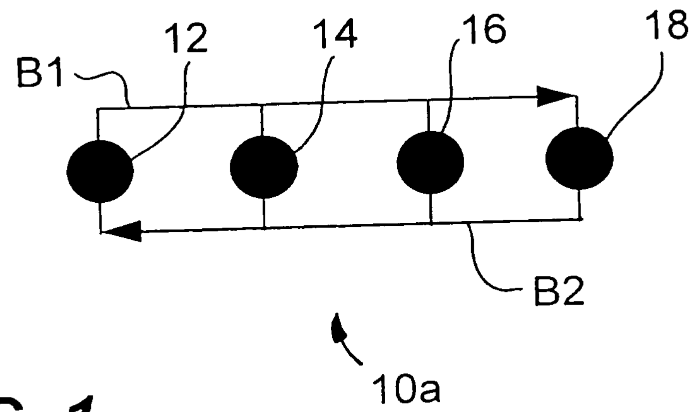



FIG. 1

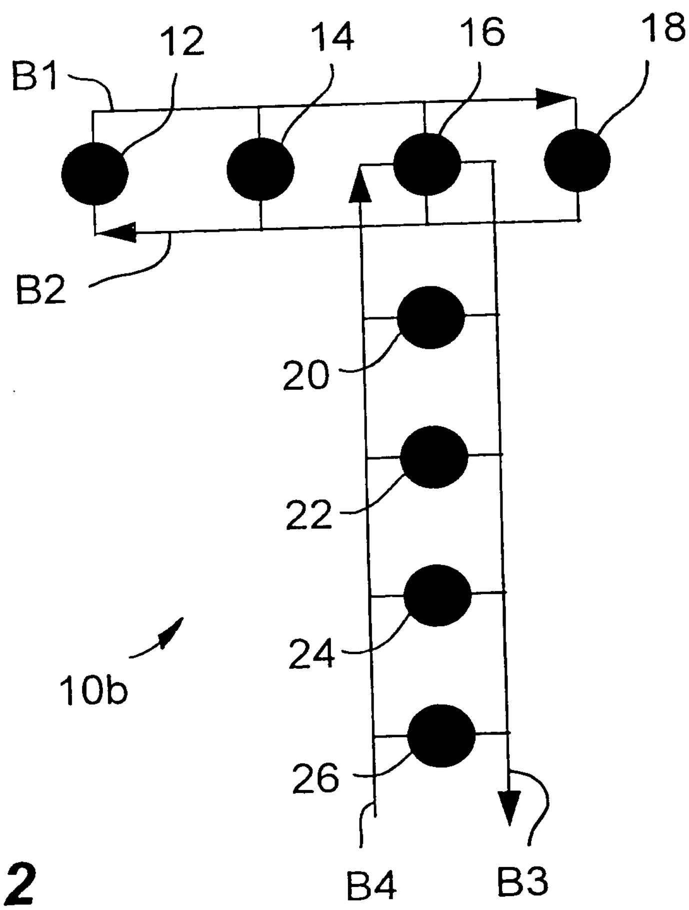



FIG. 2

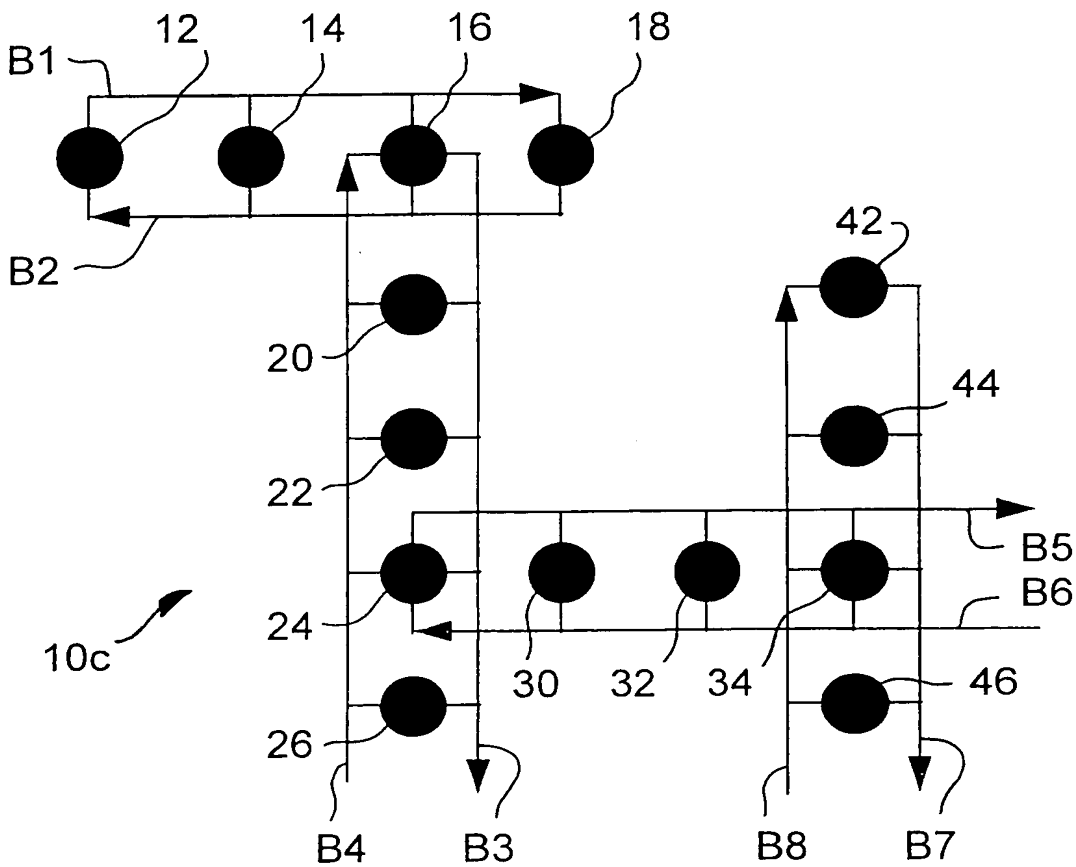
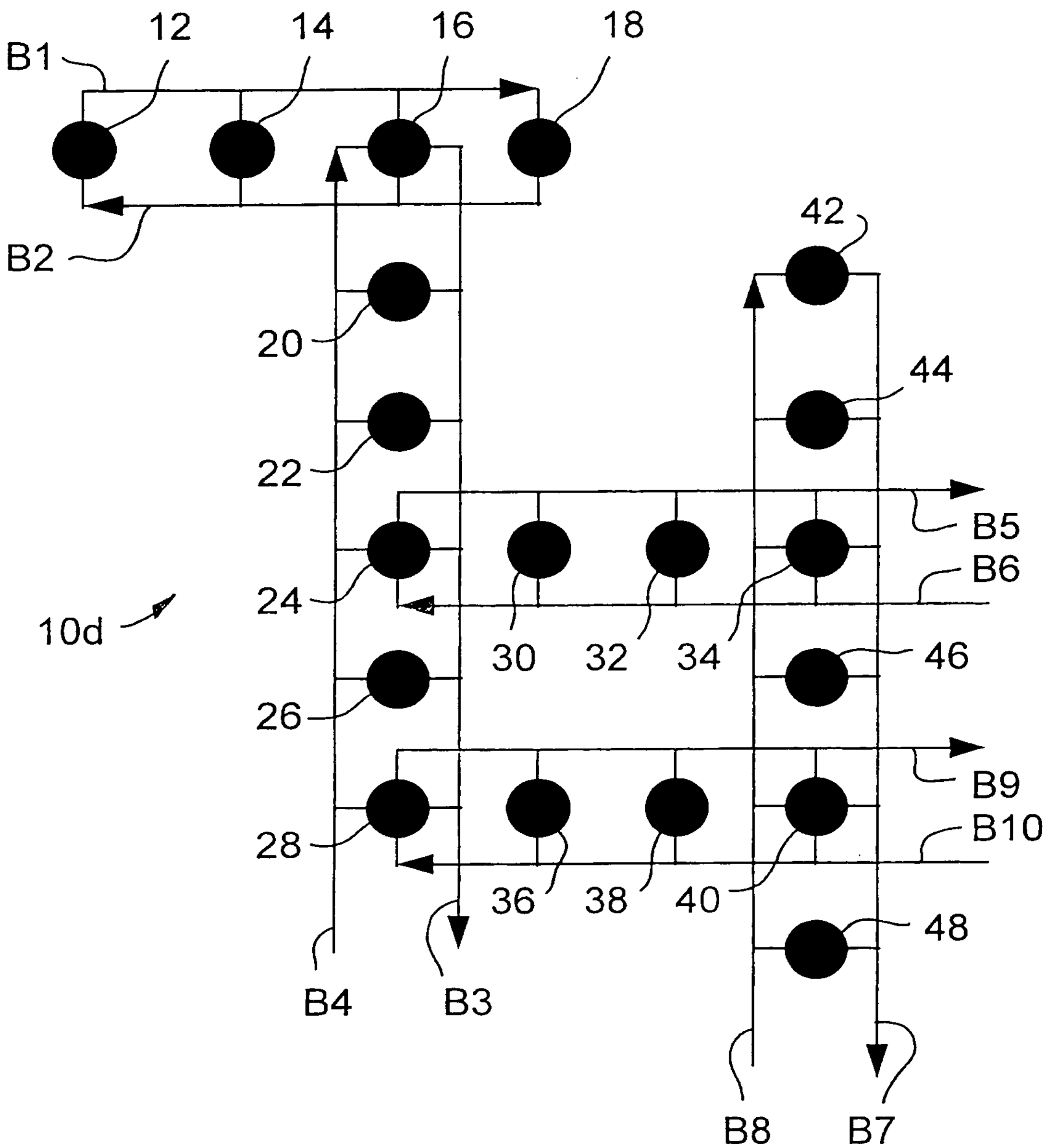
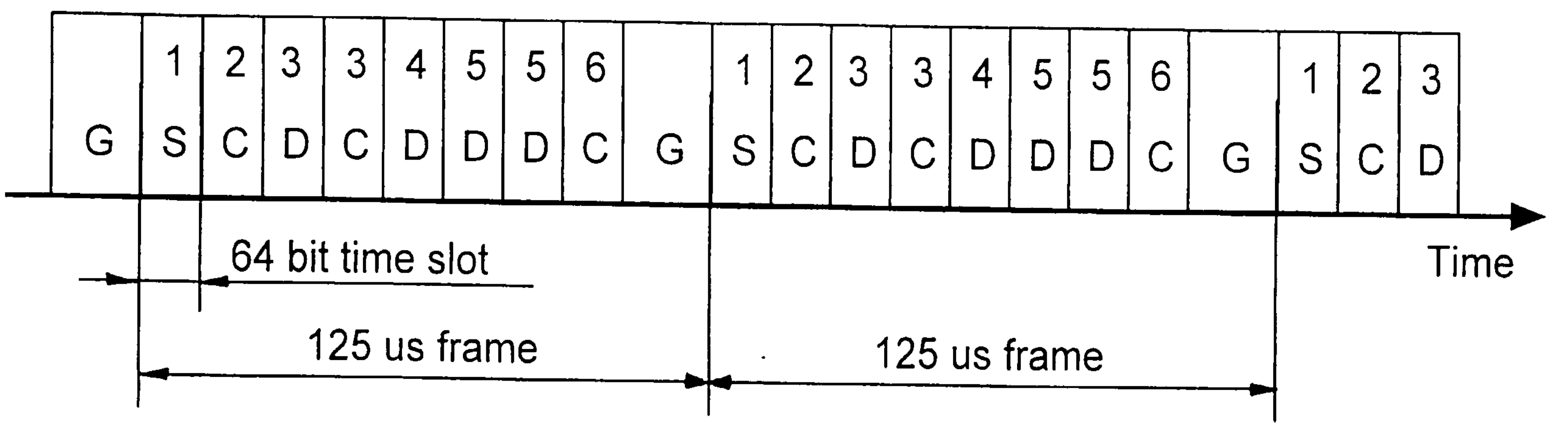



FIG. 3



B1
12
14
16
18
B2
42
20
44
22
B5
B6
24
30
32
34
46
10d
26
B9
B10
28
36
38
40
48
B4
B3
B8
B7


*FIG. 4*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2 C
3 D
3 C
4 D
5 D
5 D
6 C
G
1 S
2 C
3 D
3 C
4 D
5 D
5 D
6 C
G
1 S
2 C
3 D
Time
64 bit time slot
125 us frame
125 us frame

FIG. 5

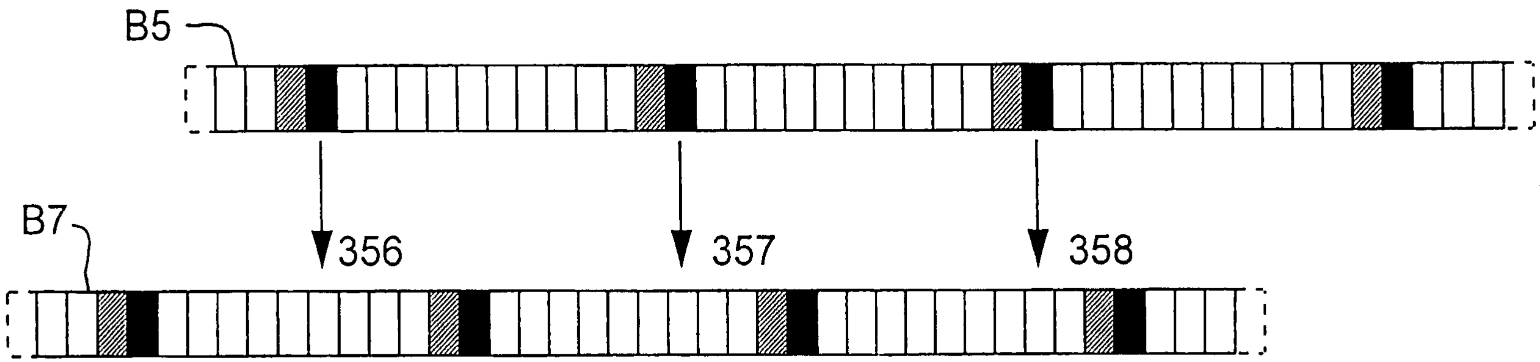


FIG. 6a

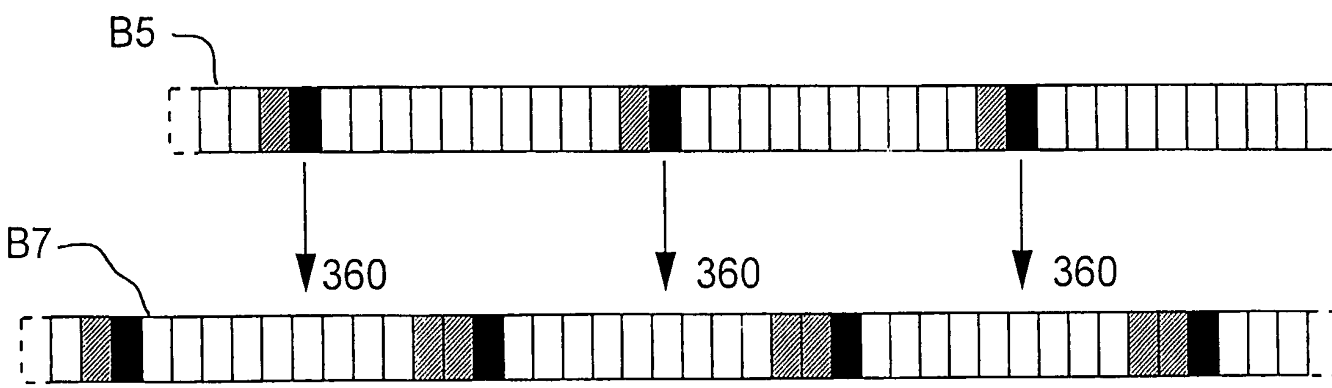


FIG. 6b

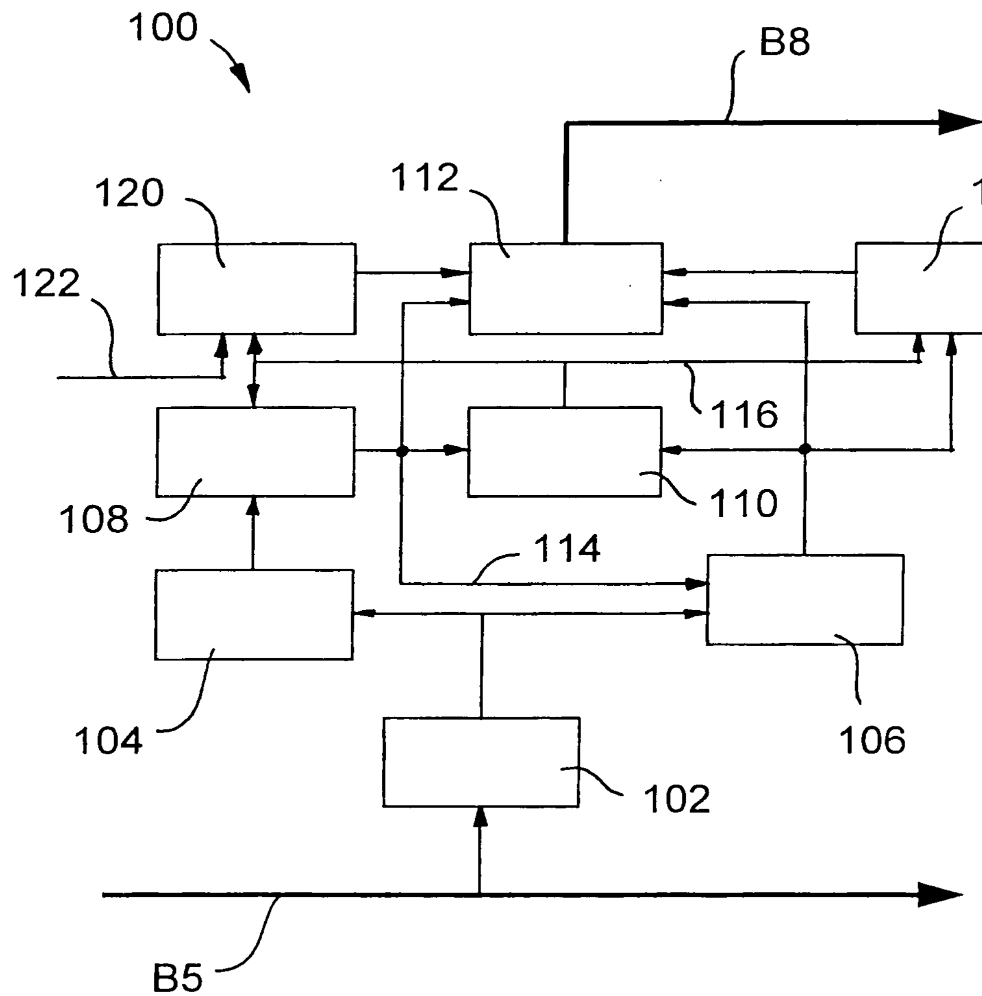


FIG. 7